# Adaptive Linear Neural Network Approach for Three-Phase Four-Wire Active Power Filtering under Non-Ideal Grid and Unbalanced Load Scenarios

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**Abstract:** This paper presents the enhancements performed on the adaptive linear neuron (ADALINE) technique so that it can be applied for active power filtering purposes in a three-phase four-wire system. In the context of active power filtering, the ADALINE technique which was initially developed for a single-phase two-wire system has been further expanded to suit three-phase three-wire system. For both systems, ADALINE techniques have been reported to be effective even when the grid voltage is distorted and/or unbalanced. However, further works that study the possibility to apply ADALINE technique in a three-phase four-wire system which invariably carries unbalanced loads, are rather limited. Hence, in this work, a control algorithm (named as enhanced-ADALINE) which combines the strength of highly selective filter (HSF), ADALINE concept and averaging function is proposed, to manage harmonics mitigation by shunt active power filter (SAPF) under non-ideal grid and unbalanced load scenarios. MATLAB-Simulink software is utilized to conduct an exhaustive simulation study which includes circuit connection of SAPF in a three-phase four-wire system, design of control algorithms, and performance assessments. Benchmarking with the existing algorithm is performed to examine the benefits of using the proposed algorithm. From the analysis, simulation findings are presented and thoroughly discussed to verify design concept, capability, and relevance of the proposed algorithm.

**Keywords:** active filtering; artificial neural network; control algorithm improvement; harmonics solution; intelligent technique; simulink/MATLAB; unbalanced load scenarios

## 1. Introduction

Shunt active power filter (SAPF) is a well-recognized power electronics tool applied for mitigating harmonic currents sourced by non-linear harmonic producing loads. Its purpose is to recover sinusoidal shape and balanced property of source currents by injecting equal amount of harmonic currents in opposite phase (referred here as injection currents) to the existing harmonic currents retained in the power system. In modern days, installation of SAPF has been made compulsory due to increasing penetration of power electronics devices into power systems where they have significantly contaminated the power system with harmonic currents. SAPFs are revealed to be flexible and adaptive

where they can favorably be installed in any harmonic-contaminated power systems [1]. These are the key features of SAPFs that allow them to overcome the main limitations of traditional tuned filters which are passive and non-adaptive (fixed filtering feature), and eventually grabbed the status as the best harmonic currents solution [2]. However, the developing innovative approaches that allow SAPFs to perform at the peak of their ability have always remained a core challenge.

In this regard, progressive research works have been performed extensively to investigate and subsequently improve performance of SAPF by developing new control techniques. Generally, to manage operation of SAPF, three distinct groups of control algorithm need to be integrated in its controller: (1) harmonics extraction, (2) dc-link voltage regulation, and (3) current control algorithms [3,4]. Among the three control categories, harmonics extraction algorithms are acknowledged to be most essential because they hold the responsibility to provide the controller with reference current signal. It is worth noting that reference current signal is the main signal that guides the generation of control signals and eventually the operation of SAPF. Hence, without having an accurate reference signal as guideline, there is no way the SAPF can perform as desired.

A few popular techniques for developing harmonics extraction algorithms include synchronous reference frame (SRF) [5,6], instantaneous power (PQ) theory [7,8], Fourier transform [9,10], and artificial neural network (ANN) [11,12] techniques. Among the aforementioned techniques, harmonics extraction developed based on ANN or more specifically adaptive linear neuron (ADALINE) concept, is most reliable in providing accurate estimation of reference current [13]. In operation, ADALINE-based approaches are technically managed by a modified Widrow-Hoff (W-H) weights updating algorithm [11,14] which matches an estimated signal to an actual signal by continuously updating the weights of each neuron (sine and cosine components).

In the context of SAPF applications, an early work on ADALINE-based harmonics extraction algorithm was performed on single-phase systems [11] where it was reported to effectively manage the operation of SAPF under ideal source voltage and steady state conditions. The work has been further improved as fundamental active current (FAC)-ADALINE where it allows the controlled SAPF to work effectively under dynamic state conditions [13]. Further progressive works have been performed to expand the application of ADALINE-based approaches to address harmonic problems in three-phase three-wire systems [15,16]. For three-phase applications, the single-phase ADALINE technique can be adopted directly, i.e., by assigning similar single-phase ADALINE module across each phase of the three-phase networks. In this manner, the design efforts can particularly be reduced as similar design requirements are applied for each phase (modular structure). Performances of ADALINE-based approaches in three-phase three-wire systems have been verified (both simulation and experimentally) under sinusoidal source, balanced load, and dynamic state scenarios [16].

Nevertheless, for both single-phase and three-phase applications, to ensure effectiveness of the ADALINE-based harmonics extraction algorithm, additional implementation of synchronizer such as zero-crossing detector (ZCD) [11] and phase-locked loop (PLL) [12] is required. The purpose of the synchronizer is to match the phase of the generated reference current signal with the phase of the operating power system. Specifically, the ADALINE technique alone is for estimating either fundamental or harmonic currents and at the same time the synchronizer will coordinate the phase of the estimated currents according to the phase of the operating power system. In other words, the estimated fundamental/harmonic currents signal with the correct phase is the reference current signal needed. Indeed, the additional ZCD and PLL circuitries will complicate the structure of the ADALINE-based harmonics extraction algorithm and thus the overall control structure. Alternatively, an ADALINE-based fundamental voltage extraction algorithm [16,17] can be applied to replace the traditional ZCD and PLL. As the name indicates, this algorithm is developed by using ADALINE concept where it has a similar control structure with the ADALINE technique that is originally used for extracting fundamental/harmonic currents. This innovative algorithm is named as unified ADALINE. It contains two similar ADALINE structures: the first one for extracting fundamental voltage signal (for phase synchronization) and the second one for extracting fundamental current

signal [16]. Since both ADALINE structures are similar, hence no additional design effort is needed in developing a unified ADALINE technique.

However, from a practical point of view, the source voltage is most probably non-ideal (distorted and/or unbalanced), and thus worsens the performance of SAPF which is initially developed to operate with ideal source voltage (sinusoidal and balanced) scenarios. Owing to source voltage distortion and unbalances, the traditional ZCD and PLL may not perform as desired because their tracking ability can be degraded according to the severity of distortion and/or unbalances suffered by source voltages [18]. Meanwhile, according to the ADALINE-based fundamental voltage extraction algorithm, the synchronization phase is literally a unity representation of the source voltage, obtained by dividing the sinusoidal source voltage with its magnitude (extracted by the ADALINE algorithm) [16]. In this case, if the source voltage is distorted and/or unbalanced, the unified ADALINE (as a whole) will probably fail to work as desired [19]. Fortunately, techniques to deal with distorted and/or unbalanced source voltage scenarios have been developed such as by using adaptive notch filters (ANFs) [20] and highly selective filters (HSF) or self-tuning filters (STFs) [18,19,21]. For the purpose of generating reference current, STF has been integrated with ADALINE technique (named as STF-based ADALINE) and this innovative technique has been reported to work effectively under various distorted and/or unbalanced source voltage scenarios [19].

Hence, ADALINE-based approaches for the purpose of harmonics extraction have improved in a progressive manner, i.e., from single-phase two-wire to three-phase three-wire applications, from steady state to dynamic state operations, and from ideal to non-ideal source voltage scenarios. However, relevant studies to examine the possibility to adapt the ADALINE-based algorithm in a three-phase four-wire system which invariably carries unbalanced loads are rather limited. Nevertheless, for three-phase four-wire applications, two common techniques, i.e., SRF [22,23] and PQ theory [7,24] techniques are reported to be effective. Indeed, both of these techniques are actually modified from their respective counterparts designated for three-phase three-wire applications. Up to date, these two techniques are still most preferred for controlling the operation of a three-phase four-wire SAPF. For instance, one recent work is reported to have applied an innovative technique that utilizes the strength of the STF and SRF concept (named as STF-dq0) for controlling three-phase four-wire SAPF [22]. The STF-dq0 technique is revealed to perform effectively under non-ideal source voltage and unbalanced loads scenarios. Hence, it would be interesting to find out how other available techniques especially the ADALINE technique can be modified to suit three-phase four-wire operation. It will serve as an important alternative other than just depending on SRF and PQ theory techniques.

Therefore, in this work, the typical ADALINE-based harmonics extraction algorithm which has been applied in three-phase three-wire system is modified to suit operation in three-phase four-wire system and eventually enhanced serving as a better alternative in generating reference current signal. The proposed algorithm is named as enhanced-ADALINE, and it is developed by integrating together ADALINE concept, HSF, and averaging function. An exhaustive simulation study inclusive of circuit connection of the three-phase four-wire system, design of control algorithms, and test and analysis of findings is performed in MATLAB-Simulink environment (R2012a, The MathWorks, Inc., Natick, MA, USA). To prove design concept of the proposed algorithm, performance demonstrated by SAPF while using the proposed algorithm is examined under various non-ideal source voltage and unbalanced loads scenarios. In addition, the recent STF-dq0 algorithm is also implemented where it serves as a benchmark to gauge the ability of the proposed enhanced-ADALINE algorithm. Nevertheless, the details on STF-dq0 algorithm will not be presented in this paper as they have clearly been described in the existing literature [22].

There are five main sections in this paper. Section 2 demonstrates operation of SAPF in a three-phase four-wire system, and subsequently clarifies the control algorithms which are considered in this work. Next, in Section 3, the design concept and operation of the proposed algorithm is thoroughly described, and the important modules of the proposed algorithm are highlighted. Section 4 provides all the simulation findings of this work. The simulation findings are presented in a comparative manner which provides

a better view on achievements of the proposed algorithm. A concluding section is presented as Section 5 to summarize important findings and contributions of this work.

## 2. Circuit Connection of Shunt Active Power Filter in a Three-Phase Four-Wire System and Associated Control Algorithms

Conceptual functionality of SAPF in a three-phase four-wire system is presented in this section. To perform a mitigation operation in a three-phase four-wire system, two types of topologies can be considered for SAPF: three-phase three-leg with two dc-link capacitors split at neutral-point [23,25] and three-phase four-leg topologies [26]. In this work, a standard three-phase three-leg topology is adopted, and the circuit connection is illustrated in Figure 1. The three-phase output of the SAPF is connected to the operating power system at point of common coupling (PCC) and its neutral-point is connected to the neutral-wire $N$ of the power system. Typically, there will be an output filter interfacing between the SAPF and power system. The output filter which is commonly an inductor can potentially reduce switching ripples produced by the SAPF, allowing the desired injection current $i_{inj}$ to be accurately injected into any harmonic-contaminated power system for mitigation purposes. Additionally, in a three-phase four-wire system, due to unbalanced loads, there is a high possibility that excessive neutral current $i_N$ may be retained in the returning neutral-wire $N$. This problem can be rectified via the additional wire which links the middle-point of the two split capacitors to the neutral-wire $N$ of the power system. Note that, when SAPF performs its intended mitigation function, it will at the same time draw a small amount of current (commonly referred as dc-link charging current $i_{dc}$) from the power system to regulate its switching losses. From another point of view, the charging current is drawn to maintain a constant dc-link voltage so that a steady output voltage can be produced at the ac side of the SAPF. As for the load configuration, in a three-phase four-wire system, the connected load can be a balanced three-phase load and balanced/unbalanced group of three single-phase loads. Ideally, a proper function SAPF should be able to remove harmonic and excessive neutral currents from the power system, and as a result, the source current $i_S$ which is initially non-sinusoidal will recover its sinusoidal appearance, operate with fundamental frequency and in-phase with the source voltage $v_S$, while the neutral current $i_N$ will be ideally zero.

Nevertheless, controlling a SAPF to perform mitigation function in a three-phase four-wire system is no easy task. In this work, its controller (as illustrated in Figure 1) needs to perform few inter-related functions which include extraction of fundamental component of load current $i_L$, tracking instantaneous phase (sine function) of source voltage $v_S$, estimation of $I_{dc}$ (magnitude of $i_{dc}$), estimation of $I_{balance}$ (magnitude of balancing current), derivation of reference current $i_{S,\,ref}$, and lastly generation of gate switching pulses. It is worth noting that a typical SAPF will operate according to the characteristics of reference current signal $i_{S,\,ref}$. A good functioning SAPF is the one with the ability to produce the desired injection current $i_{inj}$ and concurrently maintain its dc-link capacitor voltage at constant level and voltage balance across each capacitor voltage (if more than one capacitor is employed). Hence, as an overall, the reference current signal $i_{S,\,ref}$ will need to contain complete details on the power system's harmonics for harmonic cancellation, the power system's operating phases for synchronized operation, amount of dc-link charging current for regulation of dc-link voltage, and amount of balancing current for voltage balancing of split capacitors.

This paper will solely discuss the process to generate reference current signal in which the ADALINE concept is applied. Particulars of the control process are provided in Section 3. Nevertheless, for a SAPF to work, other algorithms are also required to be implemented in its controller as illustrated in Figure 1. In this regard, to maintain voltage balance of split capacitor and constant overall dc-link voltage, a simple proportional-integral (PI) technique [23,27] is adopted. Meanwhile, to convert the reference current signal into gate switching pulses, a standard hysteresis band current control (HBC) technique is adopted [23,28]. Both PI and HBC are adopted because they are the most straightforward control techniques available to perform the aforementioned functions [3].
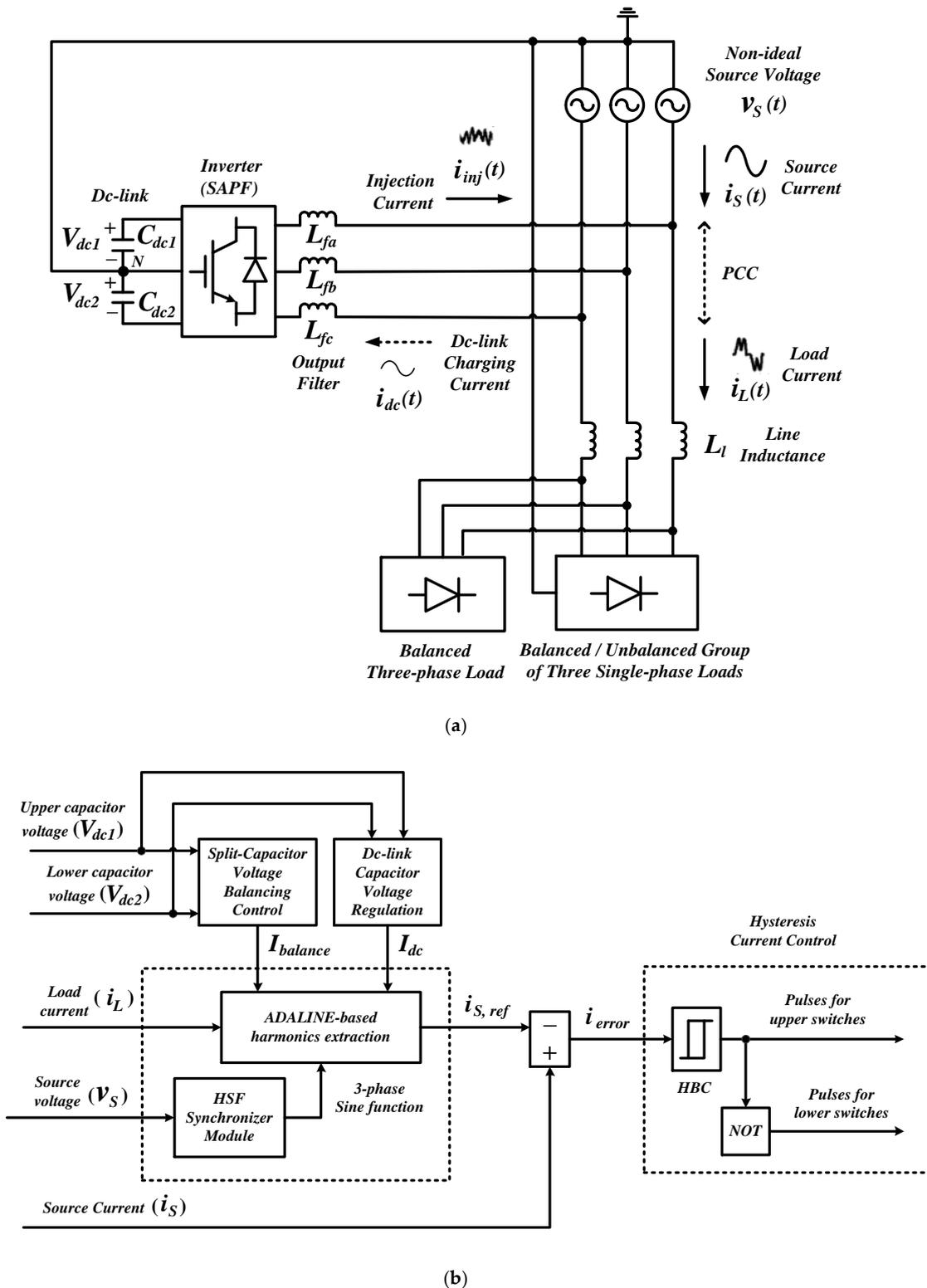
(**a**)



(**b**)

**Figure 1.** Shunt active power filter (SAPF) in a three-phase four-wire system: (**a**) connection of power circuits and (**b**) control algorithms applied.

## 3. Design Concept and Operation of Enhanced-ADALINE Algorithm

The particulars of the proposed enhanced-ADALINE algorithm will be covered in this section. As mentioned in Section 1, the proposed algorithm is formed by modifying the existing ADALINE

algorithm applied for a three-phase three-wire system, and is enhanced by the addition of HSF and averaging function.

### 3.1. Working Principle of ADALINE Module

Figure 2 provides a block diagram showing the control process of a generalized ADALINE module. According to ADALINE concept, a modified W-H weight updating technique is applied to continuously update two weight factors $W$ ($W_{1\_sin}$ for sine and $W_{1\_cos}$ for cosine) of the fundamental component. The overall updating process performed by the W-H weight updating technique is as follows:

$$W(updated) = W(current) + \frac{\gamma e_c Y}{Y^T Y},\tag{1}$$

where $W = \begin{bmatrix} W_{1\_sin} \\ W_{1\_cos} \end{bmatrix}$ represents the weight factor, $Y = \begin{bmatrix} sin(\omega t) \\ cos(\omega t) \end{bmatrix}$ represents the fundamental sine and cosine components, $e_c = i_L - i_{Lfund\_est}$ is the error that resulted between the measured load current $i_L$ and estimated $i_{Lfund\_est}$ signals, and $\gamma$ is the learning rate.
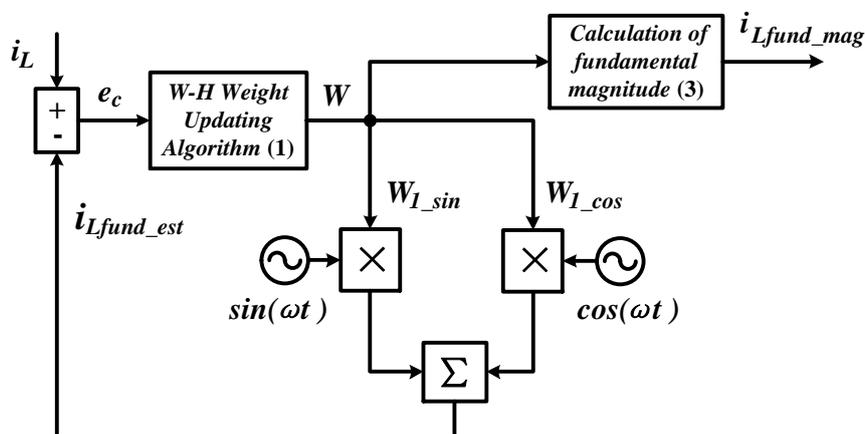


**Figure 2.** Control structure of a generalized adaptive linear neuron (ADALINE) module [11,19].

In each updating loop, $e_c$ is first computed to update the weight factors which will be applied in the subsequent loops. At the same time, $i_{Lfund\_est}$ will be updated approaching the characteristic of $i_L$ which reduces the resulted error $e_c$. After a few iterations, the estimated $i_{Lfund\_est}$ will form according to the fundamental component of $i_L$. However, updating only two weight factors for the fundamental component cannot completely remove the resulted error $e_c$ because $i_L$ also contains harmonic components. Hence, to minimize this problem, suitable learning rate $\gamma$ in the range of zero to one ($0 < \gamma < 1$) is added. Anyhow, the best $\gamma$ value reported for fundamental current estimation is 0.0006 [16,19]. Note that a fully updated $i_{Lfund\_est}$ will have the following expression.

$$i_{Lfund\_est} = W_{1\_sin} sin(\omega t) + W_{1\_cos} cos(\omega t).\tag{2}$$

Once $i_{Lfund\_est}$ is fully updated, the weight factors ($W_{1\_sin}$ and $W_{1\_cos}$) will be applied to compute the magnitude of the fundamental component $I_{Lfund\_mag}$ according to the following approach.

$$I_{Lfund\_mag} = \sqrt{W_{1\_sin}^2 + W_{1\_cos}^2}.\tag{3}$$

### 3.2. Working Principle of HSF Synchronizer Module

Figure 3 provides a block diagram showing the control structure of an HSF synchronizer module. As the name indicates, the synchronizer module is developed by expanding the function of the existing

HSF concept [18] so that it can track the operating phase of the source voltage $v_S$ and then transform it into a synchronization signal $sin(\omega t + \theta)$.
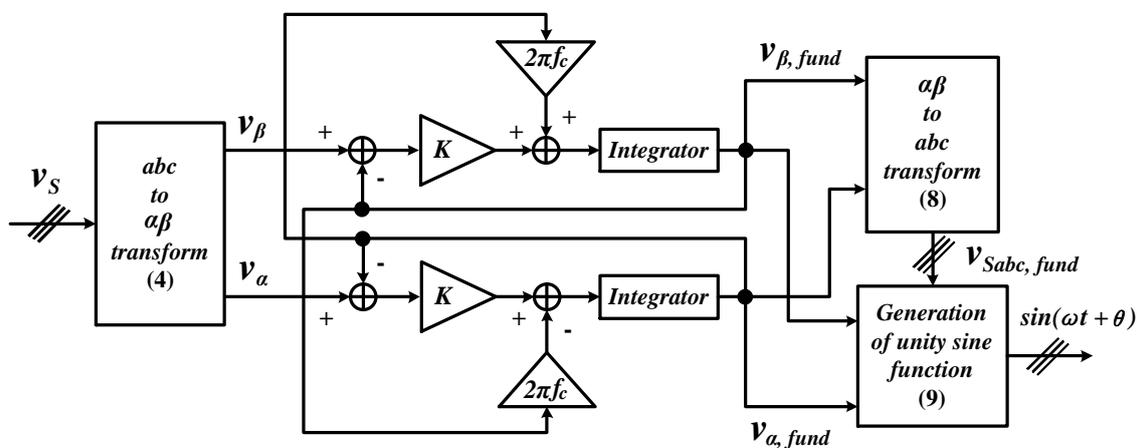


**Figure 3.** Control structure of a highly selective filter (HSF) synchronizer module.

The generation of synchronization signal is performed in two operating domains (three-phase *abc* and two-phase $\alpha\beta$ domains) involving the use of Clarke's transformation. In two-phase $\alpha\beta$ domain, fundamental component of source voltage $v_S$ is extracted, and then in three-phase *abc* domain, the extracted fundamental component is transformed into synchronization signal. First, by using Clarke transform matrix, the measured source voltage $v_S$ in three-phase domain is transformed into two-phase $\alpha\beta$ domain according to the following expression.

$$
\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{Sa} \\ v_{Sb} \\ v_{Sc} \end{bmatrix}. \tag{4}
$$

In two-phase $\alpha\beta$ domain, due to harmonic distortion, the following relation holds for the transformed source voltage signal $v_{\alpha\beta}$:

$$
\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} v_{\alpha,\ fund} + v_{\alpha,\ har} \\ v_{\beta,\ fund} + v_{\beta,\ har} \end{bmatrix}, \tag{5}
$$

where $v_{\alpha,\ fund}$ is the fundamental and $v_{\alpha,\ har}$ is harmonic components in $\alpha$ domain, and meanwhile $v_{\beta,\ fund}$ and $v_{\beta,\ har}$ represent the same relationship in $\beta$ domain.

At this stage, an HSF [18] is applied to remove the harmonic components ($v_{\alpha,\ har}$ and $v_{\beta,\ har}$) so as to deliver the fundamental component ($v_{\alpha,\ fund}$ and $v_{\beta,\ fund}$) to the subsequent processing stage. The overall operation of an HSF can be explained using the following expressions:

$$
v_{\alpha,\ fund} = \frac{K}{s}\left(v_\alpha - v_{\alpha,\ fund}\right) + \frac{2\pi f_c}{s}\left(-v_{\beta,\ fund}\right), \tag{6}
$$

$$
v_{\beta,\ fund} = \frac{K}{s}\left(v_\beta - v_{\beta,\ fund}\right) + \frac{2\pi f_c}{s}\left(v_{\alpha,\ fund}\right), \tag{7}
$$

where $K$ is a constant gain parameter and $f_c$ is the cutoff frequency. Analyses regarded to the selectivity of HSF have been reported in the literature [18,21], where it is revealed that the selectivity of HSF improves with smaller value of $K$. In addition, $K = 20$ and $f_c = 50$ Hz are also found to be the most suitable parameter settings for HSF [18,22]. Hence, in this work, similar settings for HSF are applied.

Subsequently, from the fundamental component obtained, inverse Clarke transform matrix as in Equation (8) is applied to revert the fundamental component in two-phase $\alpha\beta$ domain ($v_{\alpha,\ fund}$ and

$v_{\beta,\,fund}$) back to its equivalent representation in three-phase *abc* domain $v_{Sabc,\,fund}$. Finally, by using Equation (9), the resulting $v_{Sabc,\,fund}$ is converted into its unity form which serves as the synchronization signal $sin(\omega t + \theta)$.

$$
\begin{bmatrix} v_{Sa,fund} \\ v_{Sb,fund} \\ v_{Sc,fund} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{\alpha,\,fund} \\ v_{\beta,\,fund} \end{bmatrix}, \tag{8}
$$

$$
sin(\omega t + \theta) = \frac{v_{Sabc,\,fund}}{\sqrt{v_{\alpha,\,fund}{}^2 + v_{\beta,\,fund}{}^2}}. \tag{9}
$$

### 3.3. Integration of ADALINE, HSF, and Averaging Function for Generating Reference Current

Figure 4 provides a block diagram showing the particulars of the enhanced-ADALINE algorithm. As clearly illustrated, the ADALINE and HSF synchronizer modules as presented in Sections 3.1 and 3.2, respectively, are important constituents of the proposed algorithm. In the enhanced-ADALINE algorithm, three ADALINE modules are applied (one for each phase) to extract the magnitude of fundamental load current component from each phase of the three-phase system. From the extracted magnitude for each phase, the mean value is taken so that equal magnitude can be distributed to each phase to ensure balanced operation of the three-phase system. Note that this is important especially when unbalanced load is connected to the system as the load current will be unbalanced in terms of magnitude.

In addition, to further enhance ability of the proposed algorithm, an averaging function is added to filter out higher frequency elements (ripples) from the extracted magnitude. In a highly harmonic-distorted environment, the extracted fundamental magnitude is most likely to contain a high number of ripples which would require an additional filter to minimize them. In this aspect, the added averaging function will perform according to the following expression:

$$
I_{Lfund\_mag\,(average)} = \frac{1}{3T} \int_0^T \left( I_{La\,fund\_mag} + I_{Lb\,fund\_mag} + I_{Lc\,fund\_mag} \right) dt, \tag{10}
$$

where $I_{La\,fund\_mag}$, $I_{Lb\,fund\_mag}$, and $I_{Lc\,fund\_mag}$ represent the magnitude of fundamental component extracted from each phase, $I_{Lfund\_mag(average)}$ is the resulting average value, and $T$ is the period of the processed signals. At this stage, the proposed algorithm is said to be ready for generating reference current signal.

For generating reference current signal, the proposed algorithm needs to work closely with all the other algorithms in the control system. As described in Section 2, $I_{dc}$ and $I_{balance}$ are needed to regulate all dc-side voltages. In this regard, $I_{dc}$ is estimated by using a PI controller (PI$_1$) which minimizes the voltage difference $e_{v1}$ between reference dc-link voltage $V_{dc,\,ref}$ and the total instantaneous dc-link voltage ($V_{dc1} + V_{dc2}$). Similarly, another PI controller (PI$_2$) is applied to estimate $I_{balance}$ by minimizing the voltage difference $e_{v2}$ between the two split dc-link capacitors. In a mathematical manner, the dc-side voltages control approaches can be expressed as

$$
I_{dc} = k_{p1}e_{v1} + k_{i1} \int_0^t e_{v1}dt, \tag{11}
$$

$$
I_{balance} = k_{p2}e_{v2} + k_{i2} \int_0^t e_{v2}dt, \tag{12}
$$

$$
e_{v1} = V_{dc,\,ref} - (V_{dc1} + V_{dc2}), \tag{13}
$$

$$
e_{v2} = V_{dc2} - V_{dc1}, \tag{14}
$$

where $k_{p1}$, $k_{i1}$, $k_{p2}$, and $k_{i2}$ are the constant values that respectively symbolize proportional $k_p$ and integral $k_i$ gains for PI$_1$ (first PI) and PI$_2$ (second PI) controllers. The gain values are set to be 0.3, 2, 0.02, and 0.1, respectively [22].

Finally, by utilizing all the available signals, the reference current signal $i_{S,ref}$ can be generated according to

$$i_{S,ref} = \left( I_{Lfund\_mag(average)} + I_{dc} \right) sin(\omega t + \theta) + I_{balance},$$  (15)

where $sin(\omega t + \theta)$ is the synchronization signals (unity sine function) delivered by the HSF synchronizer module.
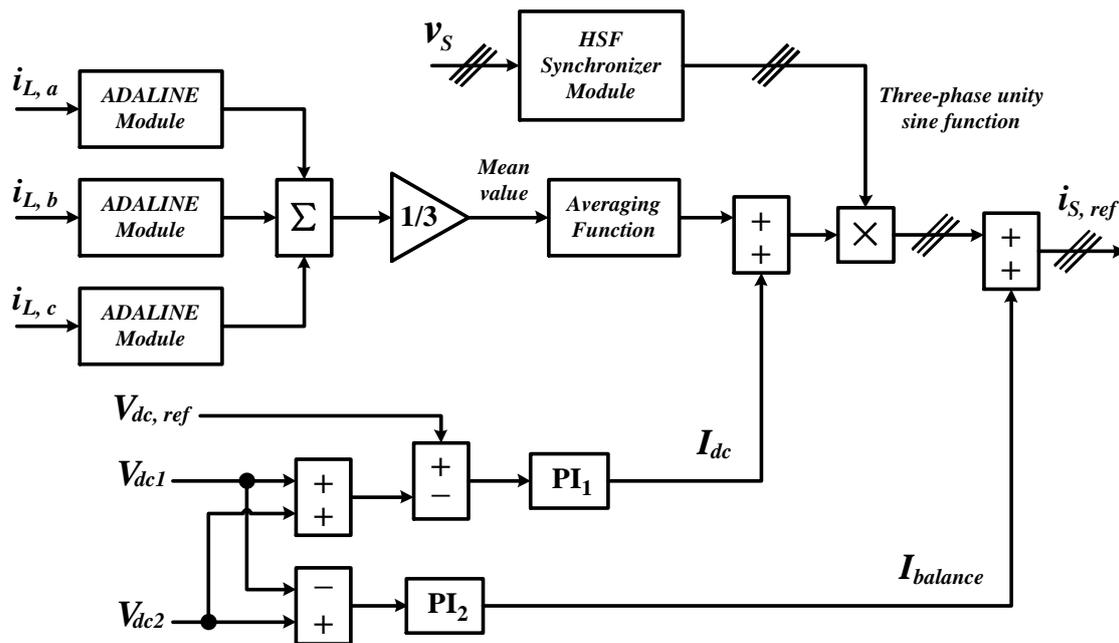


**Figure 4.** Control structure of the enhanced-ADALINE algorithm.

## 4. Results and Discussion

In this work, MATLAB-Simulink platform (R2012a) was applied to perform an exhaustive simulation study. By using basic SimPowerSystems blocks, a simulation model which consists of circuit connection of SAPF in three-phase four-wire system and the control algorithms applied was developed as in Figure 5. For the SAPF topology, a standard two-level three-leg inverter with two split capacitors of 3300 μF (each) sharing a common neutral-point was adopted. A simple 5 mH *L*-typed output filter was interfacing between the SAPF and PCC to minimize switching ripples. Meanwhile, the dc-link reference voltage was set at a total value of 880 V (440 V each). For load setting, two types of non-linear loads were considered, and the particulars are summarized in Table 1. As presented, Load A was developed by connecting three single-phase rectifier loads and a three-phase rectifier load in parallel to the power system. Meanwhile, Load B contained only three single-phase rectifier loads with a common neutral. A line inductor with the value of 1 mH was interfacing between the load and power system. Note that the unbalanced load scenarios were created by connecting different setting of single-phase rectifier load to each operating phase.
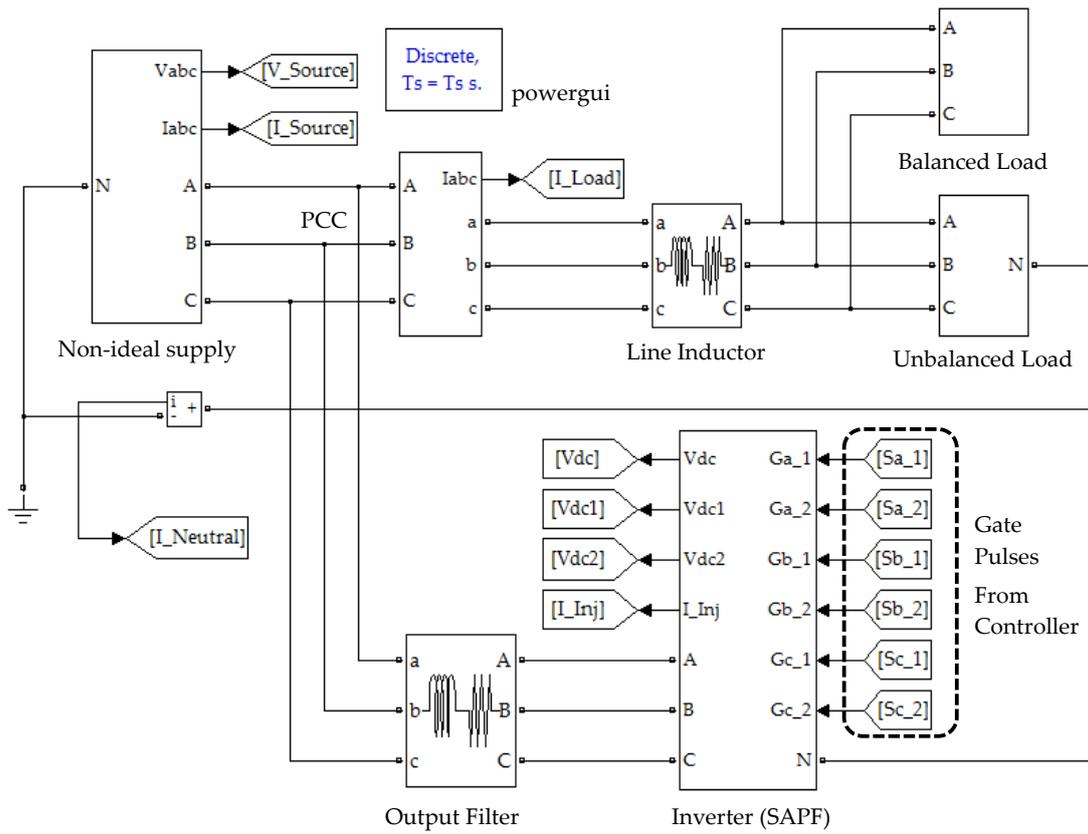
(**a**)
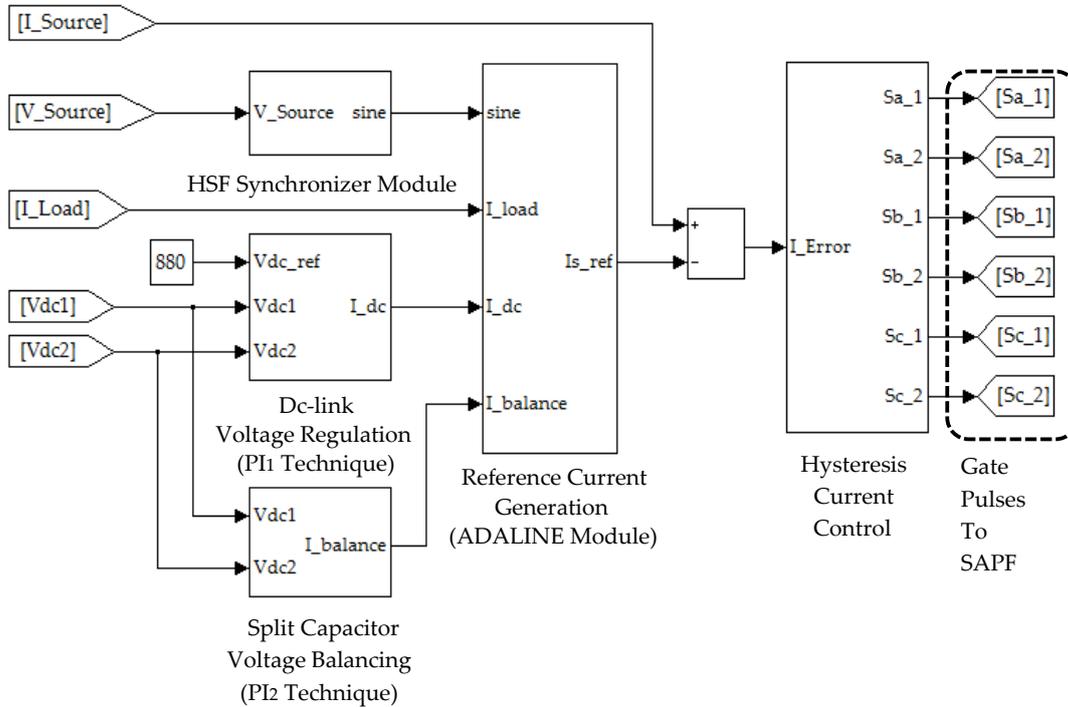


(**b**)

**Figure 5.** Simulation model of SAPF in a three-phase four-wire system: (**a**) connection of power circuits, and (**b**) control algorithms that constituted the control system.

**Table 1.** Applied load setting to create unbalanced scenarios.

| Load Configuration | | | Details |
|---|---|---|---|
| Load A:<br>Three single-phase loads with a common neutral connected in parallel with a three-phase load<br>(refer Figure 5a) | Phase *a* | Uncontrolled single-phase rectifier feeding: | 80 Ω resistor and 1500 μF capacitor in parallel |
| | Phase *b* | | 20 Ω resistor and 50 mH inductor in series |
| | Phase *c* | | 40 Ω resistor and 1100 μF capacitor in parallel |
| | Phase *abc* | Uncontrolled three-phase rectifier feeding: | 30 Ω resistor and 80 mH inductor in series |
| Load B:<br>Three single-phase loads with a common neutral | Phase *a* | Uncontrolled single-phase rectifier feeding: | 20 Ω resistor and 50 mH inductor in series |
| | Phase *b* | | 80 Ω resistor and 1500 μF capacitor in parallel |
| | Phase *c* | | 40 Ω resistor and 80 mH inductor in series |

The performance of the proposed algorithm was assessed by observing the total harmonic distortion (THD) value achieved by the SAPF. According to IEEE standard 519 [29], the maximum allowable THD limit for current is 5%. In other words, harmonics mitigation by SAPF is considered to be effective only if the resulting THD value of the mitigated source current is 5% and below. The assessment is performed in comparative manner, where the performance demonstrated by the SAPF when it is controlled by the proposed algorithm is benchmarked with the performance demonstrated by the SAPF when it is controlled by the existing STF-dq0 algorithm [22]. In this regard, the STF-dq0 algorithm was developed and tested under similar test scenarios. Steady-state simulation studies were conducted, considering three non-ideal source voltage scenarios.

Scenario I: balanced and distorted source voltage.

Scenario II: unbalanced and sinusoidal source voltage.

Scenario III: unbalanced and distorted source voltage.

Figure 6 clearly shows the magnitude and waveform of the applied source voltages. Note that the source voltage applied in Scenario I contains harmonic distortion of THD = 20.80% (similar for each phase), whereas the source voltage applied in Scenario III contains harmonic distortion of THD = 16.80% for phase *a*, THD = 15.74% for phase *b*, and THD = 6.99% for phase *c*.
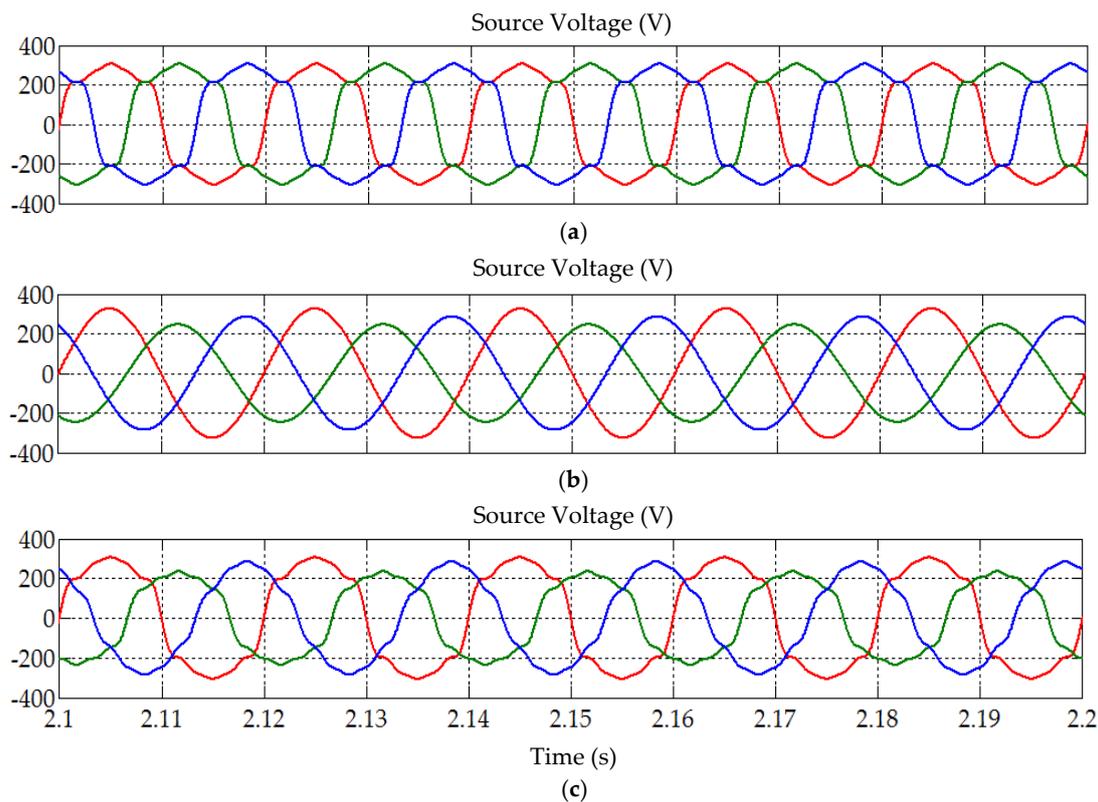
**Figure 6.** Non-ideal source voltages considered in this work: (**a**) balanced and distorted (Scenario I), (**b**) unbalanced and sinusoidal (Scenario II), and (**c**) unbalanced and distorted (Scenario III).

*4.1. Scenario I: Balanced and Distorted Source Voltage*

In Scenario I, the applied source voltage is balanced in terms of magnitude and contains an equal amount of harmonic distortion across each operating phase (refer to Figure 6a). The simulation findings obtained from this category of testing are presented in Figures 7–11. Meanwhile, to better observe the demonstrated performance, important findings are tabulated in a comparative manner, as in Table 2. First, referring to Figure 7, the enhanced-ADALINE algorithm is revealed to effectively extract the magnitude (mean value) of fundamental load current. Note that only the mean value is presented. The mean value is obtained by first adding the magnitude of fundamental load current in each operating phase, and then divides the total summation by three. As illustrated in Figure 4, the mean value is the key component needed for generating reference current, thus must be accurate. From Figure 7, without integrating the averaging function, a significant peak-to-peak oscillation (ripples) can be observed at the extracted mean value (approximately 1 A for Load A and 0.8 A for Load B). Meanwhile, by integrating the averaging function, the extracted mean value does not exhibit any significant ripples, which indicates a more accurate result.

Next, from Figures 8 and 10, the findings revealed that both enhanced-ADALINE and STF-dq0 algorithms are effective in directing their respective SAPF in mitigating the harmonics generated by Loads A and B under Scenario I. For both unbalanced load conditions, the highly distorted source currents which are mitigated by both algorithms have recovered the desired sinusoidal wave-shape with THD values (refer to Table 2) below the 5% harmonic limit. Nevertheless, as indicated in Table 2, the THD values demonstrated by the enhanced-ADALINE algorithm (1.01–2.59%) are lower than that demonstrated by the STF-dq0 algorithm (1.50–3.41%). Moreover, it is also clear from the findings that the high neutral currents that resulted from unbalanced connection of single-phase loads (both Loads A and B) were minimized. In other words, both enhanced-ADALINE and STF-dq0 algorithms are effective in removing excessive neutral currents.
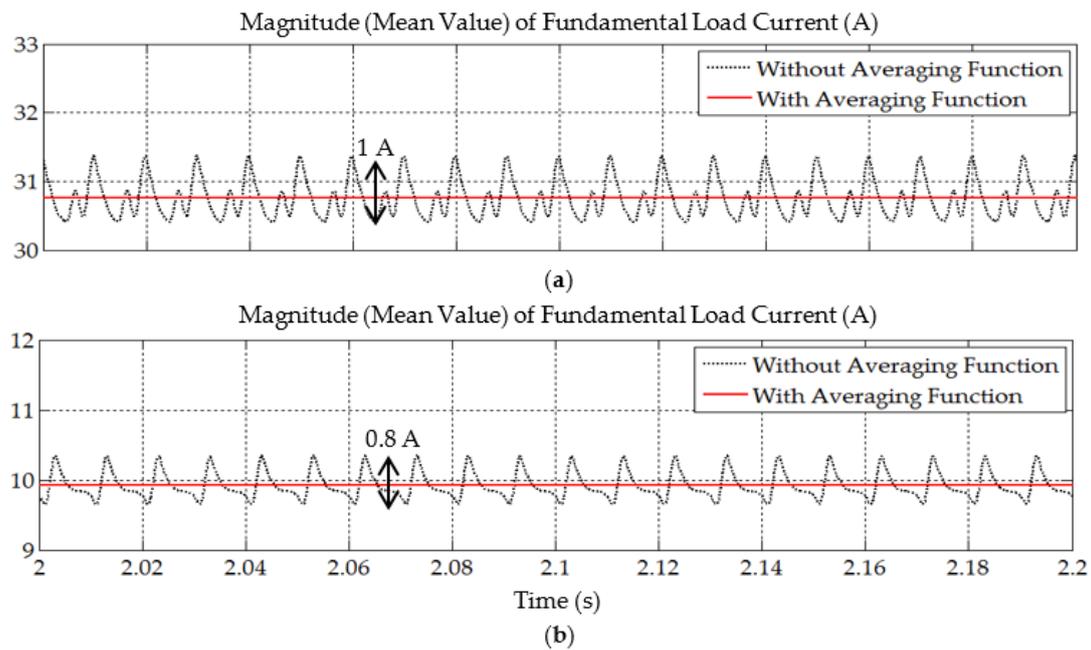
**Figure 7.** Simulation result obtained under Scenario I, showing the magnitude (mean value) of fundamental load current extracted by the enhanced-ADALINE algorithm with and without integrating Averaging function: (**a**) Load A and (**b**) Load B.

**Table 2.** Summary of performance parameters demonstrated by the enhanced-ADALINE and STF-dq0algorithms under Scenario I.

| Performance Parameter | Load A | | | Load B | | |
|---|---|---|---|---|---|---|
| | **Phase *a*** | **Phase *b*** | **Phase *c*** | **Phase *a*** | **Phase *b*** | **Phase *c*** |
| Before installing SAPF | | | | | | |
| THD (%) | 34.46 | 18.60 | 45.46 | 35.29 | 123.90 | 33.65 |
| Phase difference (°) | 13.90 | 13.10 | 12.20 | 10.40 | 10.10 | 9.00 |
| PF | 0.917 | 0.957 | 0.889 | 0.927 | 0.618 | 0.936 |
| After installing SAPF (controlled by enhanced-ADALINE algorithm) | | | | | | |
| THD (%) | 1.29 | 1.01 | 1.49 | 1.72 | 2.59 | 2.12 |
| Phase difference (°) | 0.30 | 0.30 | 0.50 | 0.40 | 0.20 | 0.90 |
| PF | 0.999 | 0.999 | 0.999 | 0.999 | 0.999 | 0.999 |
| After installing SAPF (controlled by STF-dq0 algorithm) [22] | | | | | | |
| THD (%) | 1.66 | 1.50 | 2.01 | 1.90 | 3.41 | 2.55 |
| Phase difference (°) | 0.40 | 0.30 | 0.60 | 0.50 | 0.30 | 1.10 |
| PF | 0.999 | 0.999 | 0.999 | 0.999 | 0.999 | 0.999 |

Furthermore, for both unbalanced load conditions, the large phase differences between the source voltage and current were also reduced by both algorithms. This directly indicates that both algorithms are able to synchronize operation of the SAPF with the connected power system under Scenario I. Nevertheless, the enhanced-ADALINE algorithm demonstrated a better synchronization performance by providing a lower phase difference value. As a result, in-phase operation of the source current and voltage can be achieved, and this provides a near to unity power factor (PF) of 0.999. Therefore, as an overall, the enhanced-ADALINE algorithm provides a better mitigation performance in comparison to the STF-dq0 algorithm.

**Figure 8.** Simulation results obtained under Scenario I for Load A, showing source voltage $v_{Sabc}$, load current $i_{Labc}$, injection current $i_{injabc}$, source current $i_{Sabc}$, and neutral current before and after mitigation, demonstrated by SAPF while applying the (**a**) enhanced-ADALINE and (**b**) STF-dq0 algorithms.



**Figure 9.** Simulation result obtained under Scenario I for Load A, showing the overall dc-link voltage $V_{dc}$, and individual voltage of each split capacitor $V_{dc1}$ and $V_{dc2}$, demonstrated by SAPF while applying the enhanced-ADALINE algorithm.
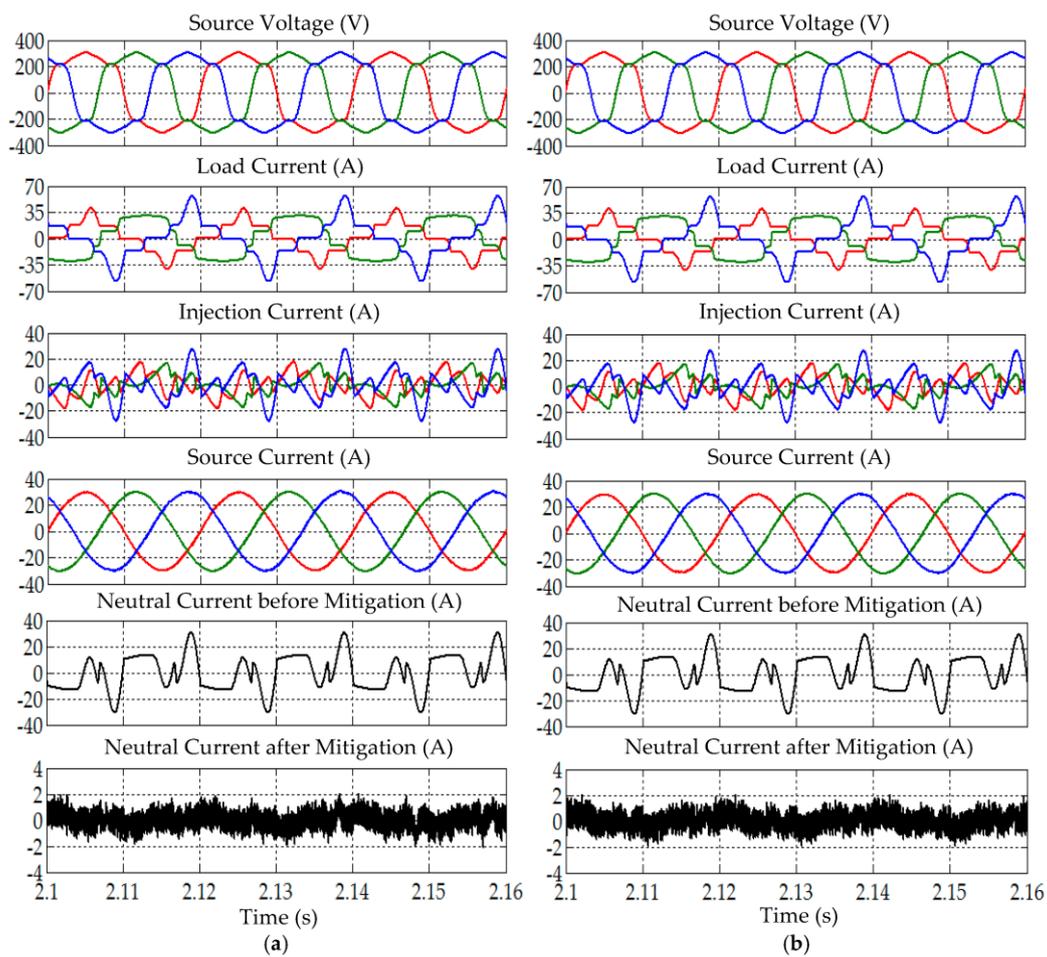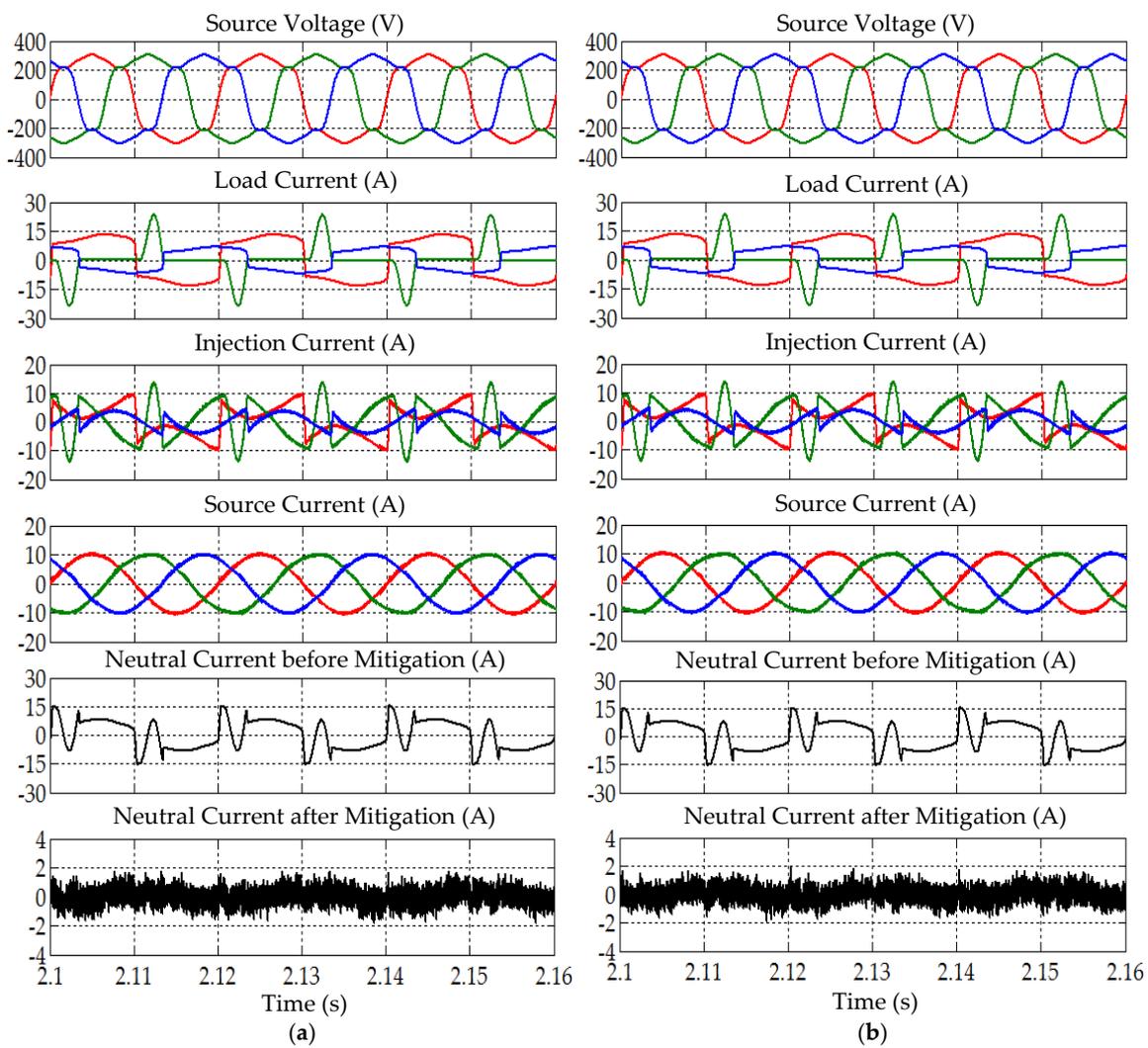
**Figure 10.** Simulation results obtained under Scenario I for Load B, showing source voltage $v_{Sabc}$, load current $i_{Labc}$, injection current $i_{injabc}$, source current $i_{Sabc}$, and neutral current before and after mitigation, demonstrated by SAPF while applying the (**a**) enhanced-ADALINE and (**b**) STF-dq0 algorithms.
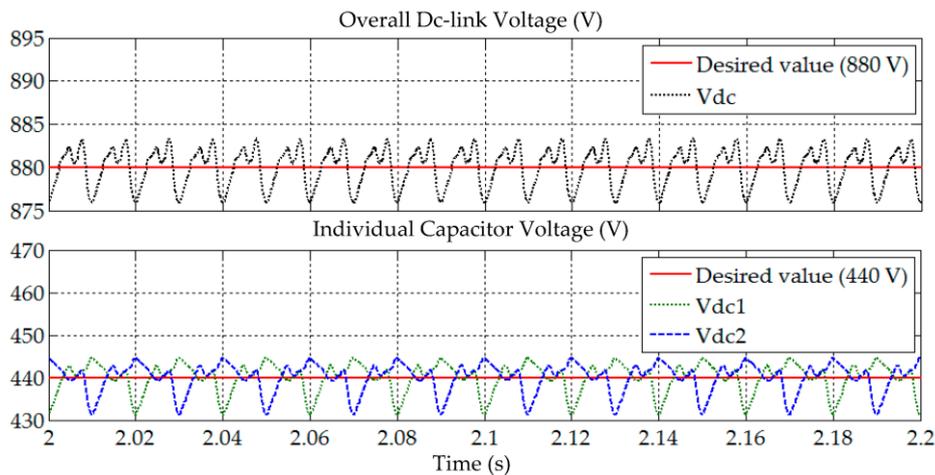


**Figure 11.** Simulation result obtained under Scenario I for Load B, showing the overall dc-link voltage $V_{dc}$, and individual voltage of each split capacitor $V_{dc1}$ and $V_{dc2}$, demonstrated by SAPF while applying the enhanced-ADALINE algorithm.
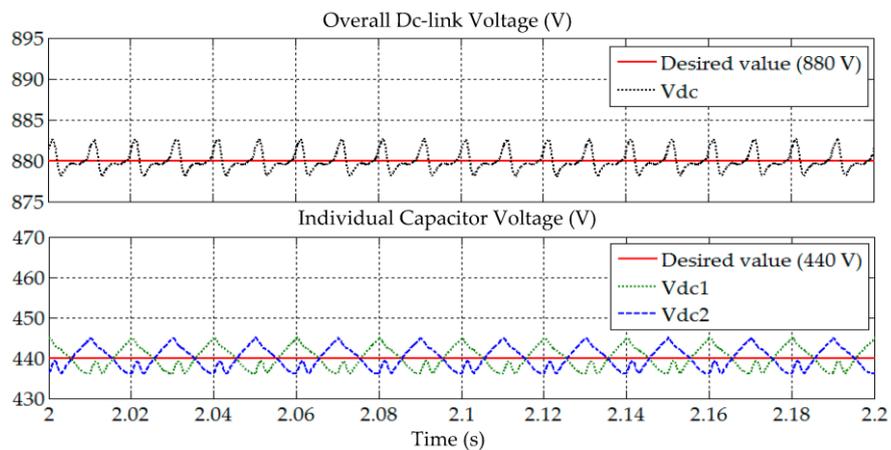
In the context of SAPF, other than its mitigation performance, it is also crucial to make sure that its dc-link voltage is correctly regulated. Figures 9 and 11 provide the related results. From both figures, SAPF controlled by the enhanced-ADALINE algorithm is able to continuously maintain its dc-link voltage $V_{dc}$ at the desired voltage level (880 V). Similarly, the individual voltage across each split capacitor $V_{dc1}$ and $V_{dc2}$, are equally maintained at the desired voltage level (440 V), i.e., half the value of the total dc-link voltage. Similar findings can be observed for Loads A and B. Hence, from all the results presented in this category, it can be confirmed that the enhanced-ADALINE algorithm is able to correctly manage operation of SAPF under Scenario I.

### 4.2. Scenario II: Unbalanced and Sinusoidal Source Voltage

In Scenario II, the applied source voltage exhibits a sinusoidal wave-shape, but its magnitude differs across each operating phase (refer to Figure 6b). The simulation findings obtained from this category of testing are presented in Figures 12–16. Meanwhile, to better observe the demonstrated performance, important findings are tabulated in a comparative manner, as in Table 3. First, referring to Figure 12, the enhanced-ADALINE algorithm is revealed to effectively extract the magnitude (mean value) of fundamental load current. Similarly, without integrating the averaging function, a significant peak-to-peak oscillation (ripples) can be observed at the extracted mean value (approximately 0.9 A for Load A and 0.5 A for Load B). However, by integrating the averaging function, the extracted mean value does not exhibit any significant ripples, which indicates a more accurate result.
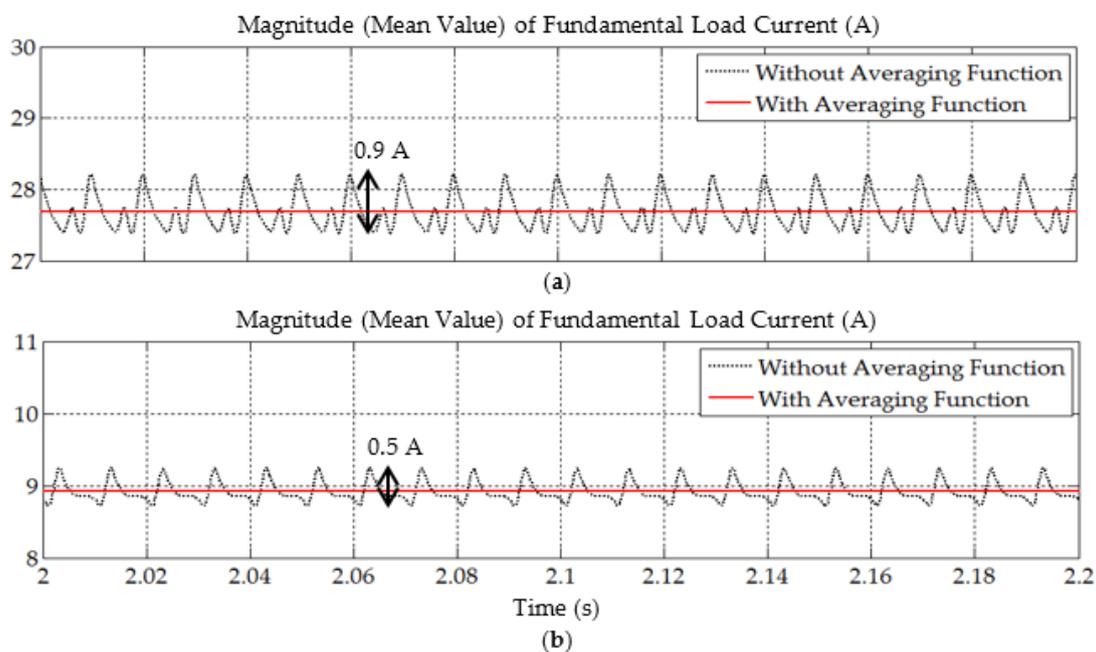


**Figure 12.** Simulation result obtained under Scenario II, showing the magnitude (mean value) of fundamental load current extracted by the enhanced-ADALINE algorithm with and without integrating Averaging function: (**a**) Load A and (**b**) Load B.

Next, from Figures 13 and 15, the findings revealed that both enhanced-ADALINE and STF-dq0 algorithms are effective in directing their respective SAPF in mitigating the harmonics generated by Loads A and B under Scenario II. For both unbalanced load conditions, the highly distorted source currents which are mitigated by both algorithms recovered the desired sinusoidal wave-shape with THD values (refer to Table 3) maintained within the 5% harmonic limit. Specifically, in terms of the recorded THD values, for Load A, the THD values demonstrated by the enhanced-ADALINE algorithm are lower than that demonstrated by the STF-dq0 algorithm. However, for Load B, the lower THD value of the enhanced-ADALINE algorithm is recorded only for phase *b*. Although the recorded THD values

for phases *a* and *c* are higher, the difference is actually not significant. Nevertheless, as an overall, the THD values recorded for the enhanced-ADALINE algorithm is of smaller value range, i.e., 0.88–2.63% while the THD values recorded for the STF-dq0 algorithm is of larger value range, i.e., 1.19–2.83%. Moreover, it is also clear from the findings that the high neutral currents that resulted from unbalanced connection of single-phase loads (both Loads A and B) were minimized. In other words, once again, both enhanced-ADALINE and STF-dq0 algorithms are shown to be effective in removing excessive neutral currents.
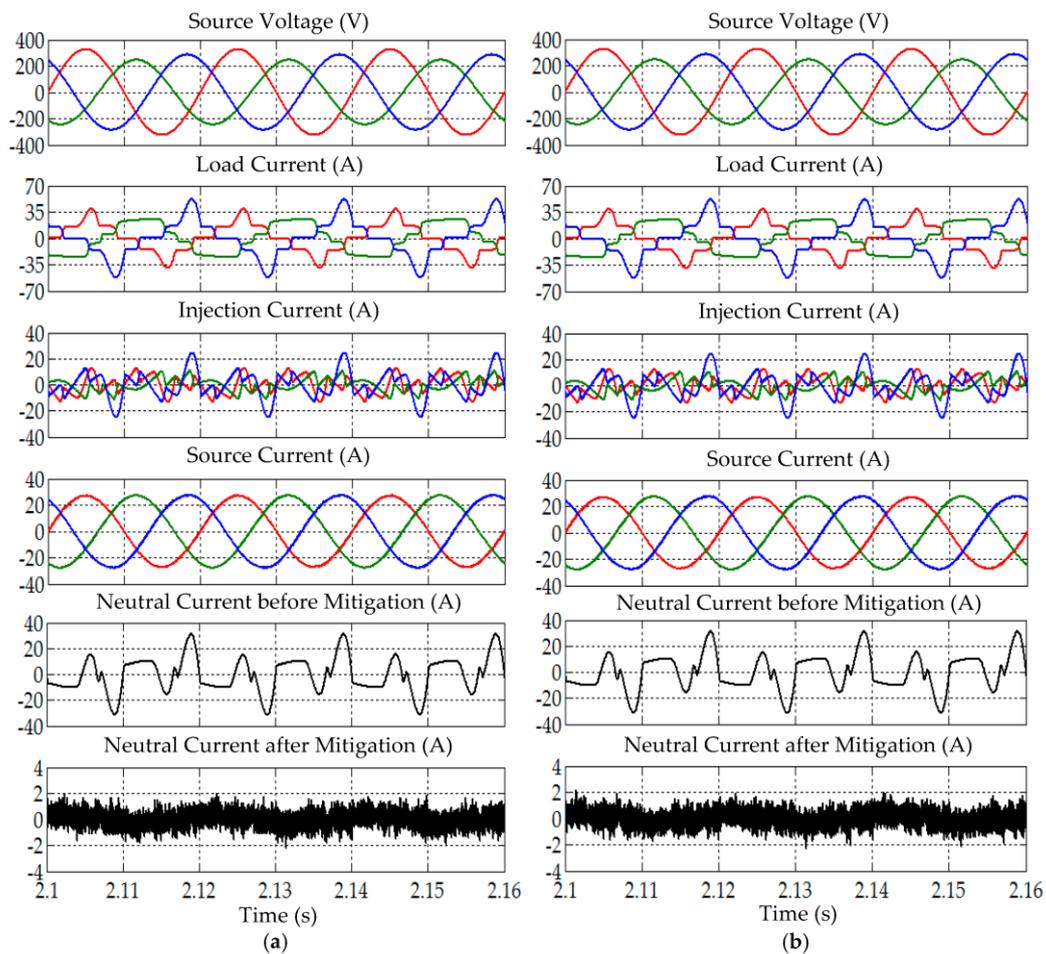
Furthermore, as tabulated in Table 3, for Loads A and B, the large phase differences between the source voltage and current were reduced by both algorithms. Hence, it indicates that both algorithms are able to synchronize operation of the SAPF with the connected power system under Scenario II. Nevertheless, the enhanced-ADALINE algorithm demonstrated a better synchronization performance by providing a lower phase difference value. As a result, in-phase operation of the source current and voltage is once again achieved, and this provides a near to unity power factor (PF) of 0.999. Therefore, as an overall, the enhanced-ADALINE algorithm is able to provide a better mitigation performance in comparison to STF-dq0 algorithm under Scenario II.

Similarly, the ability of SAPF to regulate its dc-link voltage is also assessed under Scenario II. Figures 14 and 16 provide the related results. From both figures, SAPF controlled by the enhanced-ADALINE algorithm is able to continuously maintain its dc-link voltage $V_{dc}$ at the desired voltage level (880 V). Similarly, the individual voltage across each split capacitor $V_{dc1}$ and $V_{dc2}$, is equally maintained at the desired voltage level (440 V), i.e., half the value of the total dc-link voltage. The findings are valid for both Loads A and B. Hence, from all the results presented in this category, it can be confirmed that the enhanced-ADALINE algorithm is able to correctly manage operation of SAPF under Scenario II.

**Table 3.** Summary of performance parameters demonstrated by the enhanced-ADALINE and STF-dq0 algorithms under Scenario II.

| Performance Parameter | Load A | | | Load B | | |
|---|---|---|---|---|---|---|
| | Phase *a* | Phase *b* | Phase *c* | Phase *a* | Phase *b* | Phase *c* |
| Before installing SAPF | | | | | | |
| THD (%) | 33.36 | 15.77 | 45.29 | 25.99 | 118.27 | 23.46 |
| Phase difference (°) | 9.20 | 11.20 | 5.60 | 15.60 | 9.80 | 13.80 |
| PF | 0.936 | 0.968 | 0.906 | 0.932 | 0.636 | 0.945 |
| After installing SAPF (controlled by enhanced-ADALINE algorithm) | | | | | | |
| THD (%) | 0.88 | 0.98 | 1.38 | 2.19 | 2.63 | 2.31 |
| Phase difference (°) | 0.10 | 0.60 | 0.50 | 1.20 | 0.40 | 0.80 |
| PF | 0.999 | 0.999 | 0.999 | 0.999 | 0.999 | 0.999 |
| After installing SAPF (controlled by STF-dq0 algorithm) [22] | | | | | | |
| THD (%) | 1.19 | 1.49 | 1.85 | 1.94 | 2.83 | 2.14 |
| Phase difference (°) | 0.10 | 0.80 | 0.70 | 1.40 | 0.40 | 0.80 |
| PF | 0.999 | 0.999 | 0.999 | 0.999 | 0.999 | 0.999 |

**Figure 13.** Simulation results obtained under Scenario II for Load A, showing source voltage $v_{Sabc}$, load current $i_{Labc}$, injection current $i_{injabc}$, source current $i_{Sabc}$, and neutral current before and after mitigation, demonstrated by SAPF while applying the (**a**) enhanced-ADALINE and (**b**) STF-dq0 algorithms.
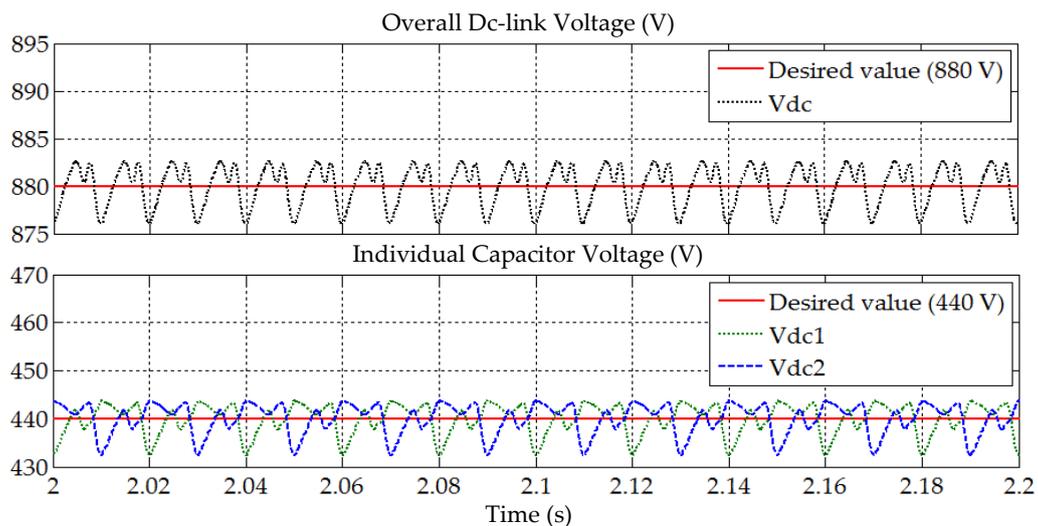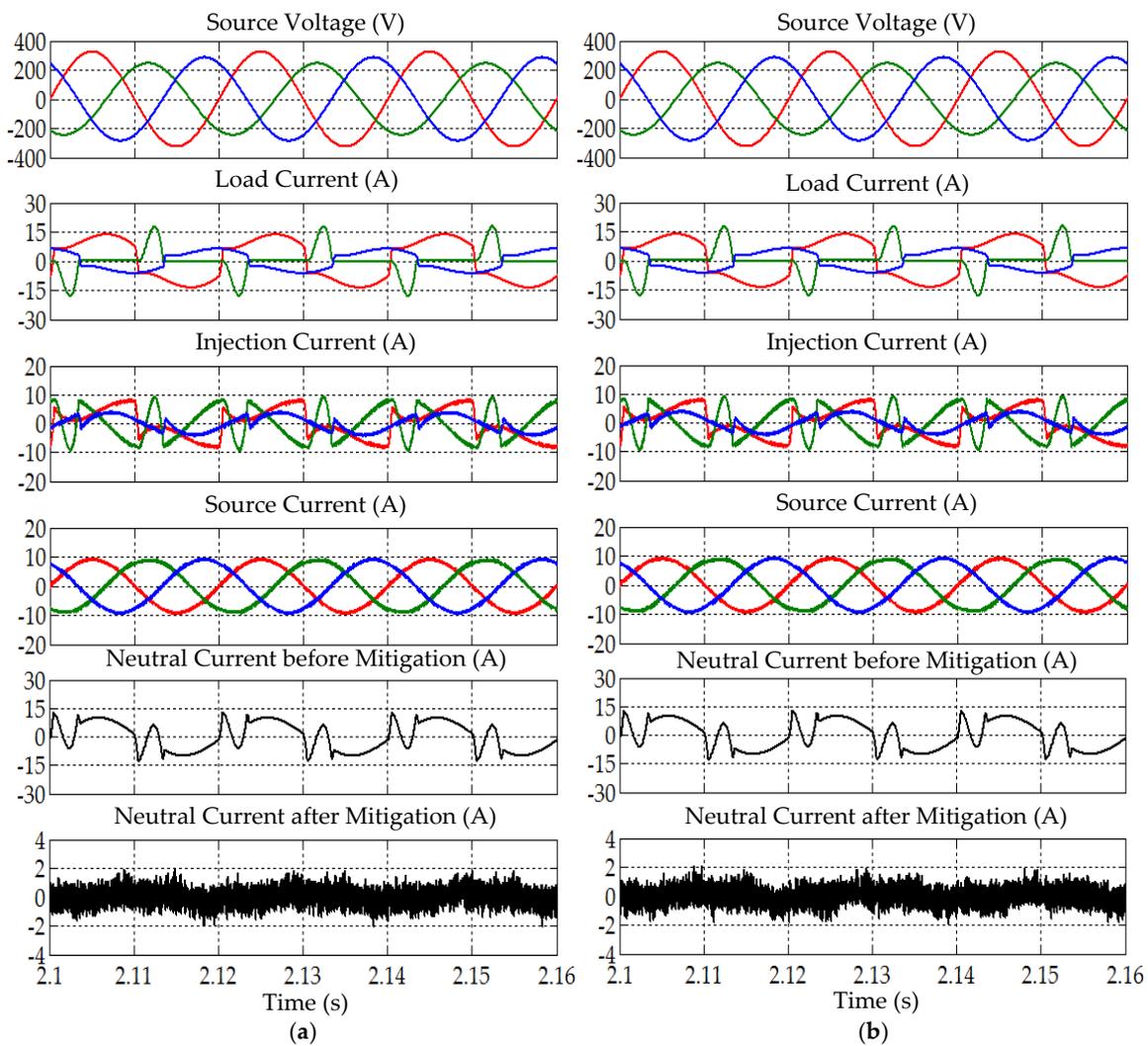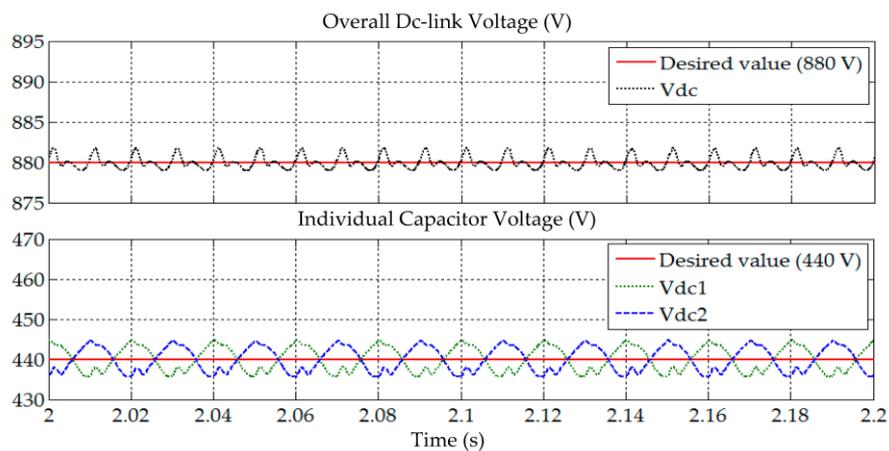


**Figure 14.** Simulation result obtained under Scenario II for Load A, showing the overall dc-link voltage $V_{dc}$, and individual voltage of each split capacitor $V_{dc1}$ and $V_{dc2}$, demonstrated by SAPF while applying the enhanced-ADALINE algorithm.

**Figure 15.** Simulation results obtained under Scenario II for Load B, showing source voltage $v_{Sabc}$, load current $i_{Labc}$, injection current $i_{injabc}$, source current $i_{Sabc}$, and neutral current before and after mitigation, demonstrated by SAPF while applying the (**a**) enhanced-ADALINE and (**b**) STF-dq0 algorithms.



**Figure 16.** Simulation result obtained under Scenario II for Load B, showing the overall dc-link voltage $V_{dc}$, and individual voltage of each split capacitor $V_{dc1}$ and $V_{dc2}$, demonstrated by SAPF while applying the enhanced-ADALINE algorithm.

### 4.3. Scenario III: Unbalanced and Distorted Source Voltage

In Scenario III, the applied source voltage is unbalanced in terms of magnitude and contains different levels of harmonic distortion across each operating phase (refer to Figure 6c). The simulation findings obtained from this category of testing are presented in Figures 17–21. Meanwhile, to better observe the demonstrated performance, important findings are tabulated in a comparative manner, as in Table 4. First, referring to Figure 17, the enhanced-ADALINE algorithm is revealed to effectively extract the magnitude (mean value) of fundamental load current. Without integrating the averaging function, a significant peak-to-peak oscillation (ripples) can be observed at the extracted mean value (approximately 1 A for Load A and 0.5 A for Load B). However, by integrating the averaging function, the extracted mean value does not exhibit any significant ripples, which indicates a more accurate result.
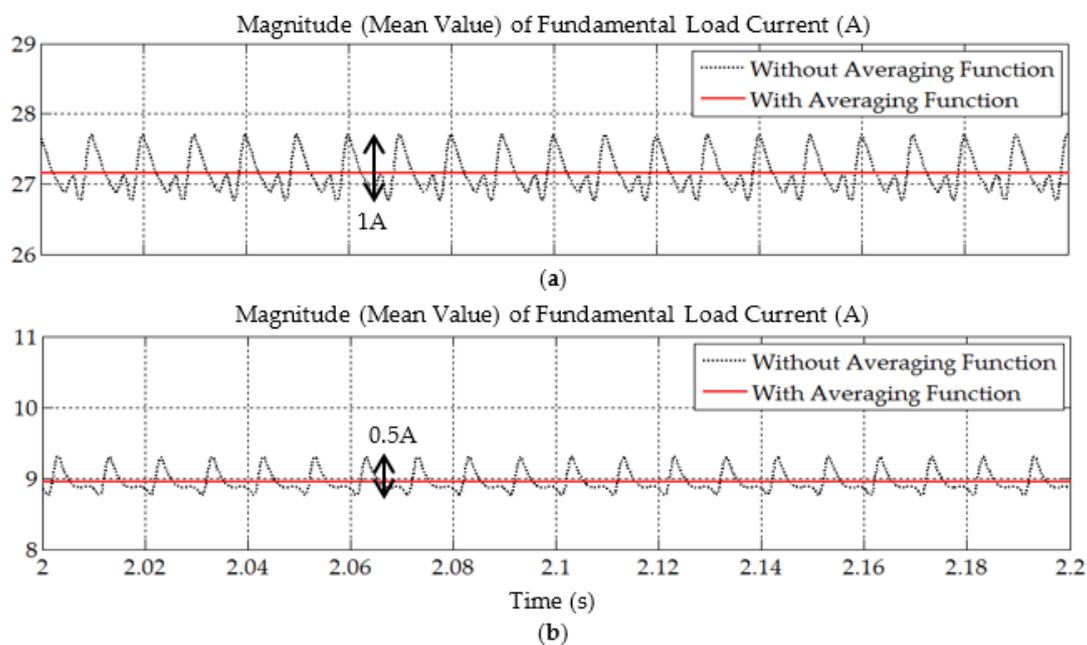


**Figure 17.** Simulation result obtained under Scenario III, showing the magnitude (mean value) of fundamental load current extracted by the enhanced-ADALINE algorithm with and without integrating Averaging function: (**a**) Load A and (**b**) Load B.

Next, from Figures 18 and 20, the findings revealed that both enhanced-ADALINE and STF-dq0 algorithms are effective in directing their respective SAPF in mitigating the harmonic currents generated by Loads A and B under Scenario III. For both Loads A and B, the highly distorted source currents, which are mitigated by both algorithms, recovered the desired sinusoidal wave-shape and the resulting THD values comply with the 5% harmonic limit, as tabulated in Table 4. Nevertheless, the THD values demonstrated by the enhanced-ADALINE algorithm (0.98–2.13%) are lower than that demonstrated by the STF-dq0 algorithm (1.66–2.92%). Moreover, it is also clear from the findings that the high neutral currents that resulted from unbalanced connection of single-phase loads (both Loads A and B) were minimized, once again showing effectiveness of both algorithms in removing excessive neutral currents.

Furthermore, as presented in Table 4, for Loads A and B, the large phase differences between the source voltage and current were reduced by both algorithms, which indicates that they are able to synchronize operation of the SAPF with the connected power system under Scenario III. Nevertheless, the enhanced-ADALINE algorithm demonstrated a better synchronization performance by providing a lower phase difference value. In this manner, in-phase operation of the source current and voltage is once again achieved, and this provides a near to unity power factor (PF) of 0.999. As an overall, the enhanced-ADALINE algorithm is able to provide a better mitigation performance in comparison to the STF-dq0 algorithm under Scenario III.

Similarly, the ability of SAPF to regulate its dc-link voltage is also assessed under Scenario III. Figures 19 and 21 provide the related results. From both figures, once again, it is clear that SAPF controlled by the enhanced-ADALINE algorithm is able to continuously maintain its dc-link voltage $V_{dc}$ at the desired voltage level (880 V). Meanwhile, the individual voltage across each split capacitor $V_{dc1}$ and $V_{dc2}$, are equally maintained at the desired voltage level (440 V), i.e., half the value of the total dc-link voltage. Similar findings can be observed for both Loads A and B. Hence, from all the results presented in this category, it can be confirmed that the enhanced-ADALINE algorithm is able to correctly manage operation of SAPF under Scenario III.

**Table 4.** Summary of performance parameters demonstrated by the enhanced-ADALINE and STF-dq0 algorithms under Scenario III.

| Performance Parameter | Load A | | | Load B | | |
|---|---|---|---|---|---|---|
| | Phase *a* | Phase *b* | Phase *c* | Phase *a* | Phase *b* | Phase *c* |
| Before installing SAPF | | | | | | |
| THD (%) | 27.74 | 18.56 | 53.32 | 33.79 | 129.01 | 27.13 |
| Phase difference (°) | 9.80 | 13.50 | 5.80 | 11.20 | 10.10 | 11.90 |
| PF | 0.949 | 0.956 | 0.877 | 0.929 | 0.603 | 0.944 |
| After installing SAPF (controlled by enhanced-ADALINE algorithm) | | | | | | |
| THD (%) | 1.45 | 0.98 | 1.87 | 1.73 | 2.13 | 1.53 |
| Phase difference (°) | 0.10 | 0.60 | 0.40 | 1.00 | 0.30 | 0.80 |
| PF | 0.999 | 0.999 | 0.999 | 0.999 | 0.999 | 0.999 |
| After installing SAPF (controlled by STF-dq0 algorithm) [22] | | | | | | |
| THD (%) | 1.91 | 1.66 | 2.34 | 2.20 | 2.92 | 2.05 |
| Phase difference (°) | 0.10 | 0.80 | 0.60 | 1.10 | 0.40 | 0.90 |
| PF | 0.999 | 0.999 | 0.999 | 0.999 | 0.999 | 0.999 |

To conclude the findings, first, in terms of the accuracy of the extracted mean value, the findings revealed that a more accurate result can be obtained by integrating the averaging function in the enhanced-ADALINE algorithm. Owing to severe distortion at the source side and unbalanced issue of the connected load, the ADALINE module alone is not sufficient to provide a ripple-free mean value, as clearly illustrated in Figure 7, Figure 12, and Figure 17. However, a ripple-free mean value of fundamental load current is highly crucial to improve accuracy of the generated reference current. Hence, in this work, an additional averaging function was integrated to remove any unwanted ripples and at the same time it improves the accuracy of the mean value. Second, in terms of harmonics mitigation performance, the findings revealed that SAPF controlled by the enhanced-ADALINE algorithm performs better in all the three scenarios as compared to the SAPF controlled by the STF-dq0 algorithm. This is supported by the smaller THD values recorded in Tables 2–4. Hence, the enhanced-ADALINE algorithm can potentially serve as an alternative to manage operation of SAPF in a three-phase four-wire system rather than just depending on the typical SRF and PQ theory techniques. Third, in the context of dc-link voltage regulation and voltage balancing, the findings revealed that the utilization of the enhanced-ADALINE algorithm does not degrade the ability of SAPF in regulating its overall dc-link and maintain its voltage balance. In other words, the enhanced-ADALINE algorithm can be integrated properly with the two PI techniques applied respectively for regulating the dc-link voltage and ensuring voltage balance of the two split dc-link capacitors. Therefore, in this work, it can be confirmed that the enhanced-ADALINE algorithm is able to correctly manage operation of SAPF in a three-phase four-wire system even if the connected grid is non-ideal and loads are unbalanced.
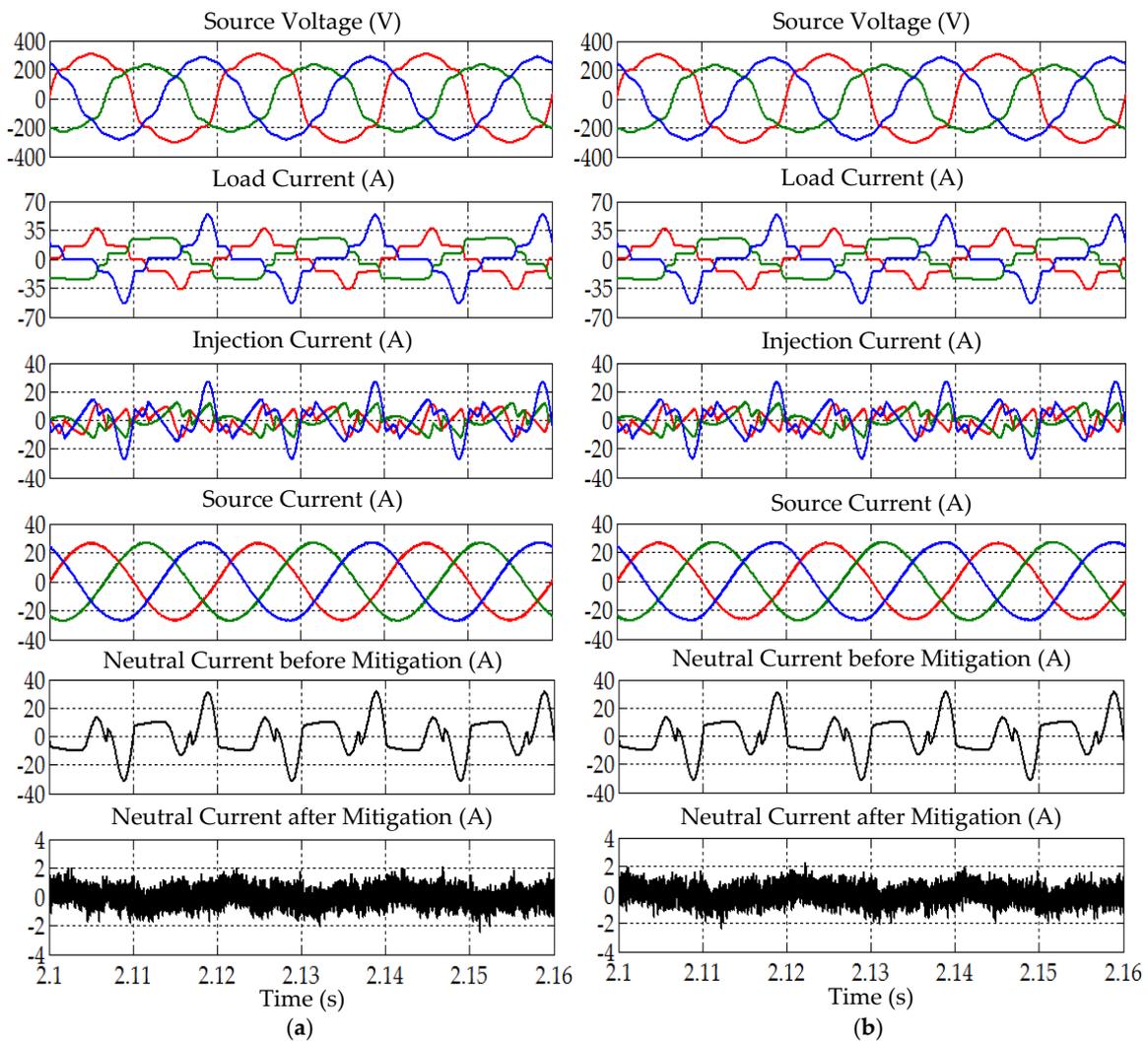
**Figure 18.** Simulation results obtained under Scenario III for Load A, showing source voltage $v_{Sabc}$, load current $i_{Labc}$, injection current $i_{injabc}$, source current $i_{Sabc}$, and neutral current before and after mitigation, demonstrated by SAPF while applying the (**a**) enhanced-ADALINE and (**b**) STF-dq0 algorithms.
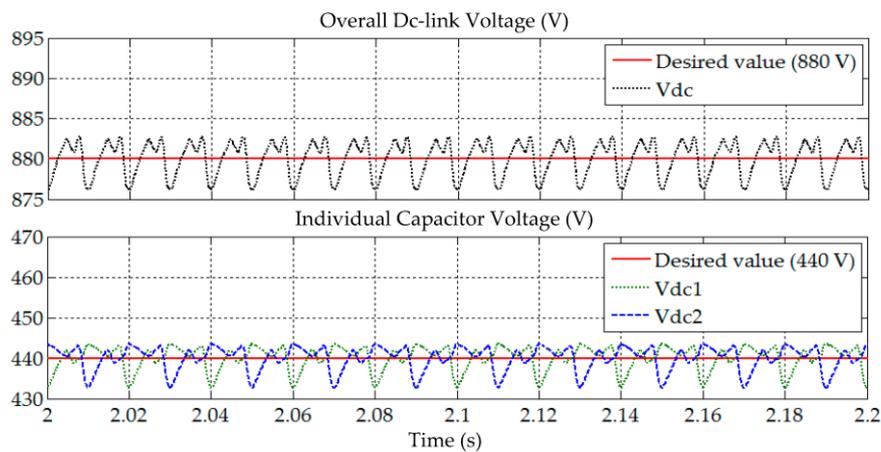


**Figure 19.** Simulation result obtained under Scenario III for Load A, showing the overall dc-link voltage $V_{dc}$, and individual voltage of each split capacitor $V_{dc1}$ and $V_{dc2}$, demonstrated by SAPF while applying the enhanced-ADALINE algorithm.
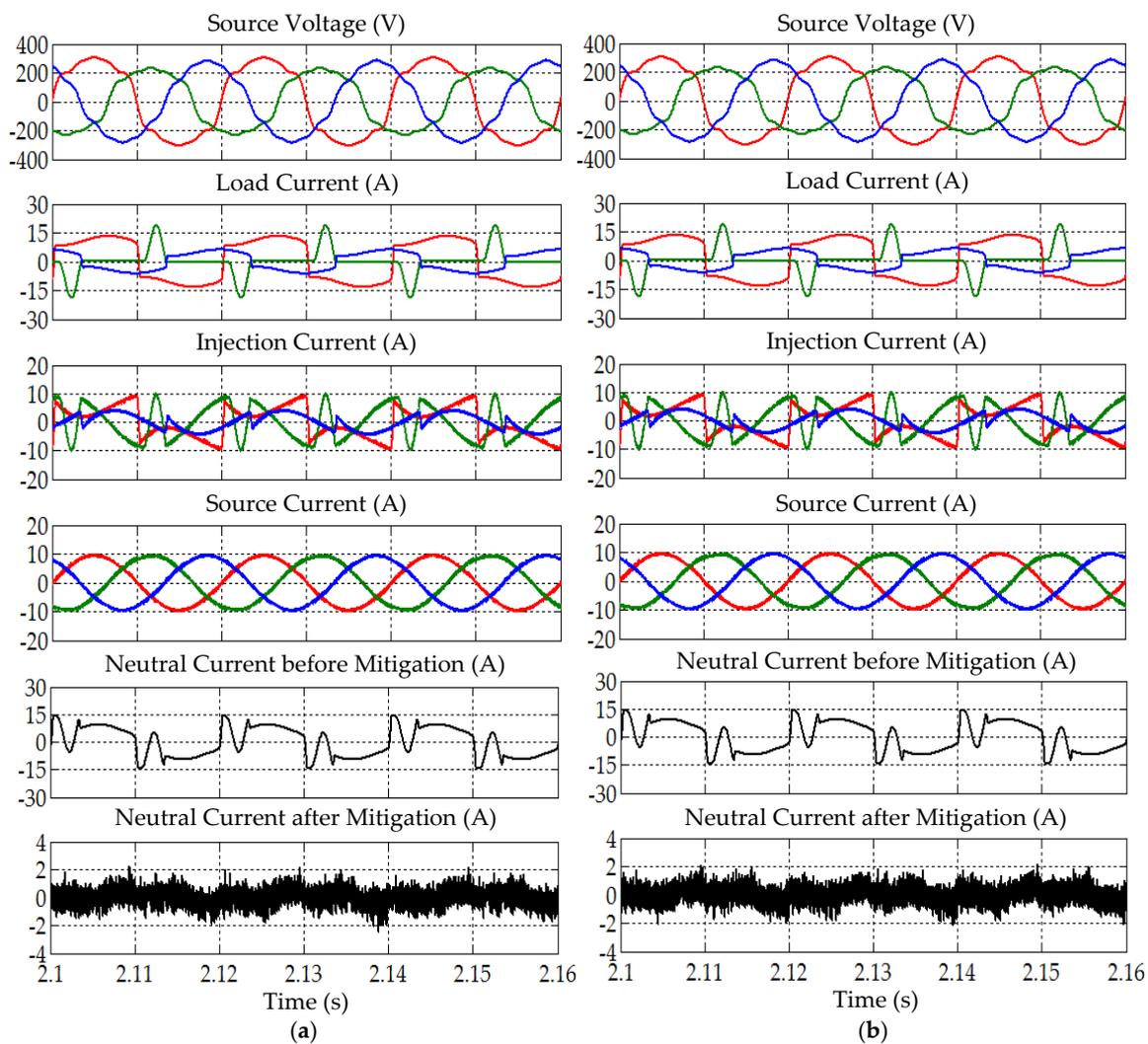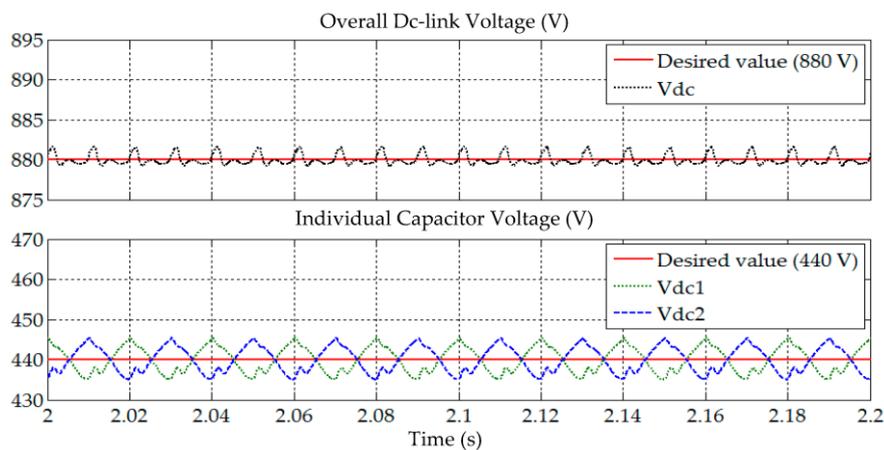
**Figure 20.** Simulation results obtained under Scenario III for Load B, showing source voltage $v_{Sabc}$, load current $i_{Labc}$, injection current $i_{injabc}$, source current $i_{Sabc}$, and neutral current before and after mitigation, demonstrated by SAPF while applying the (**a**) enhanced-ADALINE and (**b**) STF-dq0 algorithms.



**Figure 21.** Simulation result obtained under Scenario III for Load B, showing the overall dc-link voltage $V_{dc}$, and individual voltage of each split capacitor $V_{dc1}$ and $V_{dc2}$, demonstrated by SAPF while applying the enhanced-ADALINE algorithm.

## 5. Conclusions

In this paper, a control algorithm to manage SAPF's operation in a three-phase four-wire system by generating reference current signal was successfully demonstrated. The newly proposed algorithm was named as enhanced-ADALINE, where it was formed by merging three single-phase ADALINE modules, and was further enhanced by integrating an HSF synchronizer module and averaging function. Simulation tests and analyses were thoroughly performed to evaluate the performance of enhanced-ADALINE under the conditions where the grid was non-ideal (three non-ideal scenarios were considered) and the load was unbalanced (two unbalanced loads were considered). The performance demonstrated by the enhanced-ADALINE algorithm was compared to the existing STF-dq0 algorithm to gauge its capability. According to the presented findings, the enhanced-ADALINE algorithm was revealed to perform effectively despite distortion and/or unbalanced source voltage, and unbalanced connected loads. More importantly, the enhanced-ADALINE algorithm revealed to be more reliable than the existing STF-dq0 algorithm where it was able to provide a lower THD performance (0.88–2.63%) and a more synchronized operation (indicated by a lower phase difference between source voltage and current, i.e., in the range of 0.10°–1.20°). As a result, almost unity power factor was achieved. Last but not least, the enhanced-ADALINE algorithm also revealed to be effective in removing excessive neutral current, and this feature is mandatory for the harmonics extraction algorithm applied in a three-phase four-wire system. For the next research step, a laboratory prototype will be developed to validate the performance of the enhanced-ADALINE algorithm in a practical environment.

**Author Contributions:** Y.H. developed the simulation model, conducted the tests, analyzed all the important findings, and wrote the manuscript; M.A.M.R. verified the simulation study and written manuscript; A.S.A.-O. revised and finalized the drafted manuscript.

**Conflicts of Interest:** The authors declare no potential conflict of interest.

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